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EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,280	ROSSI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,25,28-32 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,16-23,25,28,29,31,32,34-37 and 39* is/are rejected.

7)☒ Claim(s) *13-15,30 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 9/9/2005 with respect to claims 1-15, 25, 28-32, 34-37 have been considered but 1-12, 25, 28, 29, 35-37 are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed 9/9/2005 with respect to claims 16-23 have been fully considered but they are not persuasive.

The Applicants asserts, "Decker teaches that a voltage is driven through the multiplexers by the amplifiers 700. Accordingly, Decker relates to a voltage mode operation and does not teach a charge mode operation as recited by claims 16 & 19."

In response, the Examiner respectfully points out that Decker teaches another embodiment having circuit configuration as disclosed in Figs. 2-6 without for the differential amplifiers 700 of the CDS circuit (detailed shown in Fig. 7) so that the column-output lines may alternatively be selectively connected via switch transistors directly to the array readout lines. See Decker, col. 10, line 67 – col. 11, line 5. In view of the above, the *integrated charge* in the active pixel sensor (detailed shown in Fig. 4) is directly output to the array readout lines via switch transistors (Decker, col. 11, lines 5-22). Thus, the Examiner submits that Decker meets the limitations of claims 16-23 as set forth below.

Claim Objections

3. Claim 1 is objected to because of the limitation of "a readout circuit" in line 14 of the claim. This limitation should be changed to --the readout circuit--.

Claim 13 is also objected because of the limitation of "the first bus" in line 7 of the claim. This limitation should be changed to --the second bus-- to comply with the specification and drawings.

Claim 21 is also objected because of the limitation of "a un-amplified pixel output signal" in line 2 of the claim. This limitation should be changed to --a pixel output signal-- to comply with the specification and 112 first paragraph rejection as set in the previous Office Action and the currently amended independent claim 19.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 16 – 23, 31, 32, 34 & 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Decker et al (US 6,512,546 B1).

Regarding claim 19, Decker discloses a method comprising:

(a) selectively enabling a supergroup select circuit (5 to 1 Mux 212; Fig. 2) from a set of supergroup select circuits (a set of circuits inside 5 to 1 MUX driven by LINE_SEL_TOP [0..4] to enable selection of each line_top0 to line_top4 shown in Figs. 2 & 5) and a series-connected group select circuit (transistors CST0 & CTS5 connected to line_top0 shown in Fig. 5; similarly CST1 & CTS 6 connected to line_top1 and so on) from an associated set of group select circuits to electrically couple a charge mode read-out amplifier (PGA 218, col. 4, lines 1-6) to a respective set of subgroup select circuits (transistors TE0, TO0,...TO329 shown in Fig. 3);

(b) when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential charge mode manner (see Fig. 12A for sequential output; col. 10, line 67 – col. 11, line 22 and col. 13, lines 20-41) through the series connected group select circuit and supergroup select circuit to the charge mode readout amplifier (see Figs. 2, 11& 12).

(c) disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits (see Figs. 11 & 12 and col. 13, lines 20-41, wherein the group select circuits CST0-CST329 are sequentially turned on and off to sequentially isolate buses TCRL0-TCRL329 from outputting signals to the amplifier 218 right after each of the signals was read out).

It is noted that the supergroup select circuits are taken as the set of circuits inside of the TOP 5 to 1 MUX 212 only.

Regarding claim 20, see the analysis of claim 19 for repeating the same operations with respect to another series-connect group associated with the supergroup select circuit and a respective set of subgroup select circuits for the imaging device to function as disclosed (see Figs. 2, 3, 5 & 12).

Regarding claim 21, see the analysis of claim 19.

Regarding claims 22 & 23, also see the analysis of claim 19, wherein disabling the supergroup select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective sets of subgroup select circuits associated with each of the group select circuits through the supergroup select circuit and to the charge mode read-out amplifier (see Fig. 12 for sequential output of pixel signal by sequentially enabling and then disabling supergroup select circuit).

Regarding claim 31, Decker discloses an imager device comprising:

groups of image sensors (groups of even and odd columns of pixels coupled to bus TCRL0...RCL329; Figs. 3-5), each group comprising a plurality of columns (group TCRL0 comprising even column selected at transistor TE0 and odd column selected at transistor TO0) of an image sensor array;

a plurality of column select circuits (transistors TE0 and TE0; Fig. 3), each of which is coupled to an output from a column of sensors (col. 5, lines 42-56);

a plurality of group select circuits (CST0...CST329; Fig. 5), each of which is coupled via a first bus (bus line_top0....line_top4) to outputs from the column select circuits associated with a respective one of the groups (col. 6, lines 35-44);

a readout circuit (218, 22) connected to outputs of said group select circuits, the readout circuit comprising a charge mode amplifier (PGA 218; col. 4, lines 1-6);

a controller (202, 204; Fig. 2) for providing control signals to the column select circuits and the group select circuits to selectively enable the respective column select circuits and group select circuits to pass signals in a charge mode manner from the sensors to said readout circuit one sensor at a time (see Figs. 11 & 12; col. 10, line 67 – col. 11, line 5 and col. 13, lines 20-41 for sequential output of signals in a charge mode manner from pixels to the readout circuit).

Regarding claim 32, it is clear that the sensors comprise active pixel sensors (see Fig. 4; col. 6, lines 20-35 and col. 13, lines 55-56).

Regarding claim 34, Decker discloses an imager device comprising:

an array of image sensors organized into supergroups (5 supergroups indicated by line_top0 ...line_top4 coupled to 5 to 1 Mux 212; Figs. 2, 3 & 5) comprising groups (groups of even and odd columns selected at CST0...CST329; Figs. 3 & 5) of subgroups (even and odd columns selected at TE0, TO0...TE329, TO329) of image sensors;

subgroup select circuits (TE0, TO0...TE329, TO329), each of which is coupled to outputs of the sensors of a respective subgroup (see Fig. 3; col. 5, lines 42-56);

group select circuits (CST0...CST329; Fig. 5), each of which is coupled to outputs of subgroup select circuits associated with a respective one of the groups (col. 6, lines 35-44);

supergroup select circuits (a set of circuits inside 5 to 1 MUX driven by LINE_SEL_TOP [0..4] to enable selection of each line_top0 to line_top4 shown in Figs. 2 & 5), each of which is coupled to outputs of group select circuits associated with a respective one of the supergroups;

at least two group buses (TCRL0...TCRL329), each group bus coupled to outputs of the subgroup select circuits associated with a respective group (see Figs. 3 & 5);

a common output bus (line_top0...line_top4; Fig. 5) coupled to outputs of the group select circuits and to a readout circuit (218, 220; Fig. 2), the readout circuit configured to amplify signals received from the image sensors (col. 4, lines 1-6);

a controller (202, 204) for providing control signals to the image sensors to produce a readout signal and to the supergroup select circuits, group select circuits, and subgroup select circuits to selectively enable the respective supergroup, group, and subgroup select circuits to pass output signals in a charge mode manner from the image sensors to the readout circuit one sensor at a time (see Figs. 11 & 12; col. 10, line 67 – col. 11, line 5 and col. 13, lines 20-41 for sequential output of signals in a charge mode manner from pixels to the readout circuit).

Regarding claim 39, see the analysis of claim 34, wherein "a first bus for each group coupled to the outputs of the associated subgroup select circuits" is indicated by each of buses TCRL0...TCRL329 shown in Fig. 5.

Regarding claims 16-18, see the analyses of claims 19-21, wherein each subgroup select circuit (transistors TE0, TO0,...TO329 shown in Fig. 3) coupled to a plurality of pixels (a column of pixels).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 7-12, 25, 28, 29, 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Decker et al (US 6,512,546 B1) in view of Takahashi et al (US 4,551,634).

Regarding claim 1, Decker teaches an apparatus comprising all limitations as analyzed in claims 34 and 39. Furthermore, Decker teaches a first isolation circuit (each of selection/isolation circuits containing transistor CST0...CST329) coupled to each first bus (each of buses TCRL0...TCRL329; Fig. 5; col. 6, lines 35-44). However, Decker does not teach that the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage.

Takahashi teaches a multiplexing circuit in which a third transistor (23-x) is added in addition to selection transistors (21-x and 22-x) to clamp the voltage level of each non-selected channel (isolated bus) to ground so that mutual interference such as noise, crosstalk between

neighboring selected and non-selected channels are prevented. See Takahashi, Fig. 2, col. 1, lines 45-55 and col. 3, line 15 – col. 4, line 15.

Therefore, it would have been obvious to one of ordinary skill in the art to improve signal integrity of the imaging apparatus in Decker by implementing a switch (i.e., a transistor) in the first isolation circuit for selectively connecting the first bus to a predetermined voltage (i.e., 0V ground) to eliminate mutual interference between neighboring buses as taught by Takahashi.

Regarding claim 2, it is clear in Decker that the sensors comprise active pixel sensors (see Fig. 4; col. 6, lines 20-35 and col. 13, lines 55-56).

Regarding claim 3, Decker discloses a second bus (line_top0...line_top4) coupled to the outputs of the group select circuits and the readout circuits (see Figs. 2, 3 & 5).

Regarding claim 7, Decker also discloses that each group select circuit comprises a transistor switch (transistor CST0 for group TCRL0, and so on; Fig. 5) with a respective gate terminal for receiving a control signal (sel_in_top; Fig. 5) from the controller, wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the first bus (line_top0...line_top4), and when the switch is turned off the group select circuit is disabled from passing signals from the associated subgroup select circuits to the first bus. See Figs. 5 & 12; col. 13, lines 20-41.

Regarding claim 8, it is clear in Decker that each subgroup select circuit comprises a transistor switch (transistor TE0 for even column selection, TO0 for odd column selection; Fig. 3) with a respective gate terminal for receiving a control signal (EVEN, ODD; Fig. 3) from the controller, wherein when the subgroup select circuit switch is turned on, the subgroup select circuit is enabled to pass signals from an associated subgroup of sensors, and when the subgroup select circuit switch is turned off the subgroup select circuit is disabled from passing signals from the associated subgroup of sensors to the first bus. See Decker, col. 5, lines 42-56.

Regarding claim 9, it is also clear in Decker that the controller (202, 204) is configured for generating the control signals to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence (see Figs. 11 & 12; col. 13, lines 20-41 for sequential enabling and disabling each group select circuit).

Regarding claim 10, Decker discloses that the controller (202, 204) is configured to provide the control signals (sel_in_top) to enable the switches (CSTO...CST329; Fig. 5) in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits (TE0, TO0...TE329, TO329; Fig. 3) associated with the particular group select circuit sequentially, one at a time (see Figs. 12A-C; col. 5, line 36 – col. 6, line 10; col. 7, lines 29-44 and col. 13, lines 20-41).

Regarding claim 11, see the analysis of claim 9.

Regarding claim 12, also disclosed is that each group select circuit comprises a pair of NMOS transistor switches (see Fig. 5 for transistors CST0 and FT0 for group TCRL0, and so on).

Regarding claim 25, see the analyses of claims 1 and 34.

Regarding claim 28, Decker discloses a step of organizing groups of subgroups of said sensors into supergroups (supergroups, each comprising subgroups/columns of pixels in 2 groups of TCRL0, TCRL5 and so on selected by a set of select circuits inside 5 to 1 Mux 212 for selecting each supergroup coupled to each line_top0 ...line_top 4 shown in Figs. 2 & 5; also see claim 19), wherein the outputs of group select circuits associated with a supergroup are connected to a respective supergroup select circuit (see Figs. 2, 3 & 5).

Regarding claim 29, Decker further discloses a step of coupling each supergroup select circuit to an associated second bus (bus at the output of 5 to 1 Mux 212; Fig. 2), wherein the readout signals from each sensor in supergroup will travel through said second bus (Figs. 2 & 5).

Regarding claims 35 & 36, as clearly taught by Takahashi, the predetermined voltage is a ground potential. See Takahashi, col. 3, lines 49-52 and col. 4, lines 10-15.

Regarding claim 37, Decker shows that the common output bus (line_top0...line_top4) is connected between outputs from the group select circuits (CST0...CST329) and the readout circuit (218). See Figs. 2, 3 & 5.

6. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Decker et al (US 6,512,546 B1) and Takahashi et al (US 4,551,634) as applied to claim 1 and in further view of Nair et al (US 6,366,320 B1).

Regarding claim 4, Decker and Takahashi do not teach that the group select circuit is approximately equal to the square root of the number of subgroup select circuits. However, as taught by Nair, an imaging device (Fig. 1) comprises a plurality of multiplexing levels, wherein the number of group select circuits (7 group select circuits 180-186) is approximately equal to the square root of the number of subgroup select circuits (50 subgroup select circuits 130-179). See Nair, col. 4, lines 3-10.

Therefore, it would have been obvious to one of ordinary skill in the art to configure the imaging device of Decker in view of Takahashi such that the number of group select circuits is approximately equal to the square root of the number of subgroup select circuits so as to optimize readout speed and helps minimize power consumption as taught by Nair, col. 1, lines 64-67.

Regarding claims 5 & 6, although Nair, Decker and Takahashi do not specifically disclose that a ratio of the number of subgroup select circuits to group select circuit is in a range

of 15:1 and 30:1 as required in claim 6 (this is also within the range of 10:1 and 40:1 required in claim 5), Nair suggests, in **col. 1, lines 29-37**, that modern imaging arrays can be very large and future arrays are expected to be even larger which requires modification on circuit design. Therefore, it would have been obvious to one of ordinary skill in the art to make a ratio of the number of subgroup select circuits to group select circuit in a range of 10:1 and 15:1 as an alternative circuit configuration depending on a size of a modern image sensor to balance readout speed.

Allowable Subject Matter

7. Claims 13-15, 30 & 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 13, the prior of record fails to teach or fairly suggest the limitations of claim 13, in combination with independent claim 1 and intervening claim 3, that includes **"a second isolation circuit coupled to each second bus for selectively isolating each supergroup from the readout circuit, the second isolation circuit comprising a switch for selectively connecting the [first] second bus to a predetermined voltage."** It is noted that the Applicant is required to comply with the objection set in section 3 above.

Regarding claims 14, 15 & 38, these claims depend from claim 13.

Regarding claim 30, the prior art of record also fails to teach or fairly suggest the limitation of claim 30, in combination with its intervening claims 28, 29 and independent claim

25, that includes **"the step of selectively applying the predetermined voltage at each second bus."**

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 7:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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